REMARKS

The Office Action includes objections to the drawings, the Abstract and written description. Changes have been made to each to accommodate the concerns expressed in the Office Action. In light of these changes, withdrawal of these objections is respectfully requested.

The Office Action also includes a rejection of claim 4 under 35 U.S.C. § 112, first paragraph, noting a minor inconsistency between the claim and the written description. This minor oversight does not justify a rejection because one skilled in the art would have understood the meaning of the claim. However, Applicants respectfully request reconsideration and allowance of the above-captioned application. Claims 1-29 are currently pending. Claims 4, and 8, have been amended.

The written description and claim 4 has been amended to clarify minor inconsistencies between the drawings and specification. The support for the claim 4 is shown in Figure 15 and specification, page 16, line 17 to page 17, line 7 for example. It is clear from the figure 15 that L*(M-FFT) refers to L M-point fast Fourier transformer. The written description has been also amended for consistency. Therefore, Applicants respectfully request the objection to the disclosure and the 35 U.S.C. §112, first paragraph, rejection be withdrawn.

Applicants respectfully traverse the 35 U.S.C. §112, second paragraph, rejection of claims 17, 24 and 25.

The Examiner stated that "the virtual pilot tones and pilot tones added upon transmission" in claims 17 and 24 lacks antecedent basis. However, "the virtual pilot tones" recited in claim 17, refer to "virtual pilot tones" in line 6. And, "the virtual pilot

tone" recited in claim 24, line 7, refers to "a virtual pilot tone" in line 6. Therefore, Applicants respectfully request that the rejection be withdrawn.

Claims 1 and 8 have been rejected under 35 U.S.C. §102(a) as allegedly being unpatentable over Cimini et al. (U.S. Patent No. 5,914,933). This rejection is respectfully traversed.

The Office Action includes the assertion that Cimini et al. discloses:

> forming a block of N coded data (ref. 119; col. 2, lines 63 - col. 3, line 17; and col. 3, line 44 - col. 4, line 56) and dividing the block into L M-sized small blocks, where N, M and L indicate integers of 1 or more, and L=N/M (ref. 31; col. 2, lines 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56); M-point inverse fast Fourier transforming the L small blocks (ref. 41; col. 2, lines 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56); combining L M-point inverse fast Fourier transformed blocks, and generating an N-sized inversely-transformed block (ref. 45; col. 2, line 63-col. 3, line 17; and col. 3, line 44-col. 4, line 56)" (see Office Action, pages 4 and 5).

The applicants respectfully disagree.

Under 35 U.S.C. §102, to anticipate a claim, the reference must teach every element of the claim. However, the Office Action does not point out how the apparatus of Cimini et al. meets the steps (b), (c) and (d) in claim 1, and the limitation recited in claim 8, lines 3-8 ("a transmission deinterleaver for firming N encoded code data into a block.,....a signal transmission interleaver for combining L M-point inverse fast Fourier transformed small blocks, thereby generating an N-sized inverse transformed block").

The Office Action includes the assertion that Cimini et al. (Fig. 2) shows M-point inverse fast Fourier transforming the L small blocks (ref. 41); combining L M-point inverse fast Fourier transformed blocks, and generating an N-sized inversely-transformed block (ref. 45). However, this assertion is contrary to what is shown in Cimini et al. Cimini et al. **does not** show inverse fast Fourier transformers (IFFT)

devices. Instead it discloses fast Fourier transform (FFT) devices 41a-41M (col. 3, lines 10-17). Moreover, the parallel-to-serial converter 45 does not function to combine L M-point inverse fast Fourier transformed blocks, and generating a N-sized inversely-transformed block. It appears that each of the M clusters is multiplexed into serial form through the parallel to serial converter 45 (col. 4, lines 51-54).

Hence Cimini et al. does not show all the limitations recited claims 1 and 8 as the applicants pointed out above, it is respectfully submitted that claims 1 and 8 are allowable.

Because claims 1 and 8 are allowable, it is respectfully submitted that all claims dependent thereon are also allowable.

Claims 4 and 11 have been rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Cimini et al. (U.S. Patent No. 5,914,933) in view of Daffara et al. (U.S. Patent No. 5,687,165). The rejection is respectfully traversed.

The Office acknowledges that Cimini et al. does not show "removing a cyclic prefix; dividing the signal sample block into L M-sized small blocks, where N, M and L are integers of 1 or more, and L=N/M; M-point fast Fourier transforming the L small blocks; combining the L M-point fast Fourier transformed small block, and decoding the detected data" see Office Action, page 6, lines 9-15. However, the Office alleges that it "would have been obvious to one of ordinary skill in the art at the time of invention to perform the reverse process in the receiver as was performed in the transmitter in order to obtain the original signal as is well-known in the art" because doing so is allegedly well known in the art as evidenced by Daffara (see Office Action, page 6, lines 18 - page 7, line 2). The applicants respectfully disagree.

First, it should be noted that the method and apparatus for transmitting OFDM signals of Cimini et al. is different from the Applicants' claimed invention as discussed above. Thus, even if the reverse process in the receiver is obvious in view of transmitter process, the steps (c), (d) and (e) in claim 4 and the recitation of, "a signal receiving deinterleaver for dividing....,; a signal receiving interleaver for interleaving the L M-point fast Fourier transformed small block, thereby generating an N-sized transform block," in claim 11, lines 6-11, are not shown in Cimini et al. or Daffara.

Because claims 4 and 11 are allowable, it is respectfully submitted that all claims dependent thereon are also allowable.

Claims 15, 16 and 21 have been rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Cimini et al. (U.S. Patent No. 5,914,933). The rejection is respectfully traversed.

The Office Action includes the suggestion that Cimini et al. shows all the limitations recited claims 15, 16 and 21 except for inserting "0" at the first position of each block after dividing the encoded data into blocks of predetermined sizes (see Office Action, page 7). Applicants respectfully disagree. There are several differences between the apparatus of Cimini et al. and the Applicants' claimed invention.

Cimini et al. does not show "a pre-processor for encoding an input data sequence and converting the encoded data **to parallel data**" as recited in claim 15, and step (a) in claim 21. Note that the Applicants' exemplary embodiment (Fig. 10) shows the encoded data, Xn is converted to parallel data through a serial-to-parallel converter 504 before the encoded data passes into a block signal domain

transformer 1000. On the other hand, Cimini et al. (Fig. 2) shows the encoded data 119 passes to the circuit 26 for dividing the encoded data into blocks of predetermined sizes, then send to a serial-to-parallel converter 31. Moreover, Cimini et al. does not show "a block signal domain transformer..., and **combining time domain signals"**. The Office states that the parallel-to-serial converter 45 operates such function. However, Cimini et al. is silent as to whether the parallel-to-serial converter 45 also contains combining function.

Furthermore, Cimini et al. does not show "a pilot signal adder for converting pilot tones, which are to be inserted at positions other than a predetermined position among the positions at which "0" has been inserted in the block signal domain transformer, into time domain pilot signals, and adding the pilot signals to the time domain signals output by the block signal domain transformer" as recited in claim 15 and step (d) in claim 21. The Office indicated that transforming pilot tones is taught by Cimini et al. (see Office Action, page 7, paragraph 17). However, it is respectfully submitted that Cimini et al. does not teach where the pilot tones are to be inserted, or the pilot tones are used for the same reason as the Applicants claim invention.

Finally, Cimini et al. does not show "a post-processor for converting the resultant signals **of the pilot signal adder to serial signals**." The Office indicated that the parallel-to-serial converter 45 provides such function (see Office Action, page 7, lines 16-17). However, the parallel-to-serial converter 45 cannot be asserted to function as both "combining the time domain signals" (see Office Action, page 7, line 12) and "converting the resultant signals of the pilot signal adder to serial signals." Moreover, Cimini et al. does not disclose the location of pilot tones (col. 4,

lines 40-49). Thus, one could not assume that the resultant signals of the pilot signal adder is converted to serial signals.

The examiner also alleges that inserting "0" at the first position of each block would have been obvious because Cimini et al. discloses the use of a guard interval and in absence of criticality (Office Action, page 8, first paragraph). The Applicants respectfully disagree.

It should be noted that inserting "0" at the first data position of each block is to avoid DC offset (page 16, lines 1-2), for instance. It has nothing to do with a guard interval. Guard intervals are designed to prevent intersymbol interference. The present invention adopts cyclic prefixes as a guard interval, which is additional evidence that the guard interval of Cimini et al. is not the same as inserting "0s" as recited in the claims.

Hence, Cimini et al. does not show all the recitations recited claims 15 and 21 as the applicants have pointed out, above, and there is no motivation to alter Cimini et al. to meet these recitations. It is respectfully submitted that claims 15 and 21 are allowable.

Because claims 15 and 21 are allowable, it is respectfully submitted that all claims dependent thereon are also allowable.

In light of the foregoing, reconsideration and allowance of the claims are respectfully requested. Should any other issue arise, the Examiner is invited to contact the undersigned at the number listed below.

Respectfully submitted,

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Attachment: Annotated Drawings